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Ad

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/316,580	05/21/99	LINN	J 87552.97R399

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MM42/0803

EXAMINER

LOKE, S

ART UNIT

PAPER NUMBER

2811

2

DATE MAILED: 08/03/99

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

Application No.  
09/316,580

Applicant(s)  
Linn et al.

Examiner  
Loke

Group Art Unit  
2811



☐ Responsive to communication(s) filed on \_\_\_\_\_

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claims

☒ Claim(s) 1-18 is/are pending in the application.

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

☐ Claim(s) \_\_\_\_\_ is/are allowed.

☒ Claim(s) 1-18 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been  
☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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1. Claims 1-18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The original specification in the parent application never discloses a substantially continuous and unbroken silicide layer and a substantially continuous and unbroken first dielectric layer as claimed in claim 1.

The original specification in the parent application never discloses the interconnected transistors are disposed in and at the upper surface of the device silicon layer as claimed in claims 1 and 7.

The specification never discloses the device silicon layer includes doped buried layers abutting the dielectric layer as claimed in claim 4.

The specification never discloses the second dielectric layer comprises diamond as claimed in claims 5 and 6.

The original specification in the parent application never discloses a substantially continuous and unbroken silicide layer is formed on the first dielectric layer as claimed in claim 7.

The original specification in the parent application never discloses a substantially continuous and unbroken second dielectric layer is disposed between the silicide layer and a device silicon layer as claimed in claim 7.

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The original specification in the parent application never discloses the homogeneous silicide layer; the device layer bonded to the silicide layer; the interconnected transistors; and the silicide layer comprises bonding material as claimed in claim 10.

The original specification in the parent application never discloses the claimed subject matters as claimed in claims 11-18.

2. The application filed 5/21/99 is objected because it introduces new matter into the disclosure. The added material which is not supported by the original parent application's disclosure is as follows:

In the specification,

[Page 3, lines 28 (Interconnected.....layer.)] 30-31 (A substantially.....dielectric layer), 31 (A substantially), page 4, lines 1 (continuous.....silicide layer), [4-5 (Interconnected.....layer.)], [7-11 (a homogeneous.....silicide layer)], page 7, lines 24-25 (continuous.....layer 406), page 8, line 19 (substantially.....layer), [32 (but.....that), page 9, lines 1- 2 (further.....together)], 22-29 (Other.....hardening.).

In the abstract,

[Lines 7-8, 15-16 (Interconnected.....layer.)], lines 10 and 12 (continuous.....layer), [lines 16-21 (a.....layer)].

Applicant is required to cancel the new matter in the reply to this Office action.

3. The disclosure is objected to because of the following informalities:

In page 6, line 24, "T'hen" is not understood.

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In page 8, line 29, "T'his" is not understood.

In page 10, line 12, it is unclear whether the handle wafer is 512 instead of 502.

In page 10, line 25, "thedevice" is not understood.

Appropriate correction is required.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4, 10, 11, 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi in view of See et al.

Moslehi shows a SOI structure in figs. 2a-2e. It comprises: an oxide layer [22] formed on a Si substrate [20]; a silicide layer [40] formed on the layer [22]; insulating layers [32, 34, 36] formed on layer [40]; a Si substrate [26] formed on layer [32].

Moslehi differs from the claimed invention by not showing transistors formed on the Si substrate.

See et al. shows bipolar and MOS transistors [28, 30] formed on a Si substrate in fig. 1.

Since both Moslehi and See et al. teach a SOI structure, it would have been obvious to have the transistors of See et al. in Moslehi because they are widely used transistor devices.

6. Claims 5, 6 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi in view of See et al., further in view of Sugimoto et al.

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Moslehi differs from the claimed invention by not showing the dielectric layer is made of diamond.

Sugimoto et al. shows the dielectric layer [2] is made of diamond in fig. 1.

Since both Moslehi and Sugimoto et al. teach a SOI substrate, it would have been obvious to have the diamond insulating layer of Sugimoto et al. in Moslehi because it prevents a heat-dissipating property from being lowered.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi in view of See et al., further in view of Iwamatsu.

Moslehi differs from the claimed invention by not showing a bonding material includes radiation-hardening dopants.

Iwamatsu shows nitrogen can be implanted into a silicon dioxide layer [2, 3] in fig. 1.

Since both Moslehi and Iwamatsu teach a SOI substrate contain silicon oxide, it would have been obvious to have the nitrogen implant of Iwamatsu in Moslehi because it prevents separation of a silicon film from the bonding face of an SOI substrate.

8. Claims 7-10 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Kameyama et al.

Ochiai discloses a semiconductor device in figs. 7-8. It comprises: a plurality of thin film transistors formed on an insulating layer [51, 55] formed on a Si substrate [50]; a resistance layer [52] formed under each of the transistors.

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Ochiai differs from the claimed invention by not showing the resistance layer is made of silicide.

Kameyama et al. shows a tungsten silicide resistor [120a] in figs. 3 and 4.

Since both Ochiai and Kameyama et al. teach a resistor, it would have been obvious to have the resistor of Kameyama et al. in Ochiai because it is a widely used resistance material.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920.

sl

July 30, 1999

STEVEN H. LOKE  
PRIMARY EXAMINER  
GROUP 2500

A handwritten signature in cursive script that reads "Steven Loke".